

**ABSTRACT**

A technique for designing a logic circuit includes specifying a model. The model including combinatorial blocks, state elements and graphical library elements. The technique  
5 maintains a data structure representative of the model, and generates an architectural model and an implementation model from the data structure. The data structure represents a descriptive net list of the model. The architectural model includes C++ code and the implementation model includes  
10 Verilog.

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